CLAIMS

What is claimed is:

(Display Device 1)

1. A display device for displaying image information according to a display signal consisting of digital signals comprising:

a display panel (110A) comprising a plurality of signal lines (DL) and a plurality of scanning lines (SL) which intersect at right angles with each other, and a plurality of display pixels (EM) with optical elements arranged near the intersecting point of the plurality of signal lines and the plurality of scanning lines;

a scanning driver circuit (120A, 120B) for sequentially applying a scanning signal to each of the scanning lines for setting the selective state of each line of each display pixel; and

a signal driver circuit (130A-G) comprising a plurality of current generation circuits (ILA, ILB, ISA, ISB, ISC-F, PXA-D); the current generation circuits comprise at least a gradation current generation circuit (21A-D) and a drive current generation circuit; the gradation current generation circuit generates a plurality of gradation currents corresponding to each of the display signal bits based on constant, predetermined reference current, and the drive current generation circuit (22A-D) generates drive current from the plurality of gradation currents based on the value of the display signal which supplies the generated drive current to each signal line.

2. The display device according to claim 1, wherein each current generation circuit sets the signal polarity of the drive current so that the drive current flows in the direction drawn from the display pixels side.

3. The display device according to claim 1, wherein each current generation circuit sets the signal polarity of the drive current so the drive current flows in the direction poured into the display pixels.

4. The display device according to claim 1, wherein each of a plurality of current generation circuits in the signal driver circuit is provided corresponding to each of a plurality of the display pixels of each scanning line of the display panel.

5. The display device according to claim 4, wherein each current generation circuit supplies the drive current simultaneously corresponding to each of a plurality of pixels of each scanning line.

6. The display device according to claim 1, wherein each current generation circuit further comprises a signal holding circuit (10, 101, 102, 103) which takes in and holds the display signal.

7. The display device according to claim 6, wherein the drive

current generation circuit generates the drive current based on the value of the display signal held in the signal holding circuit.

8. The display device according to claim 6, wherein the signal holding circuit comprises a plurality of latch circuits (LC0, LC1, LC2, LC3) which take in and hold each of the display signal bits, and outputs an output signal responsive to each bit.

9. The display device according to claim 1, wherein the drive current generation circuit comprises a switching circuit (Tr26-Tr29, Tr36-39, Tr66-69) for selecting the gradation current from the plurality of gradation currents in response to each bit value of the display signal.

10. The display device according to claim 9, the current generation circuit further comprises a signal holding circuit for taking in and holding the display signal.

11. The display device according to claim 10, wherein the signal holding circuit comprises a plurality of latch circuits which take in and hold each bit of the display signal and output an output signal responsive to each bit;

the switching circuit selects the gradation currents and generates the current drive based on the output of the plurality of latch circuits.

12. The display device according to claim 1, wherein the current value of the plurality of gradation currents have a different ratio with each other specified by 2n (n= 0, 1, 2 and 3, ...).

13. The display device according to claim 1, wherein each gradation current generation circuit comprises a plurality of gradation current transistors (Tr22-25, Tr32-35, Tr62-65) for generating a plurality of gradation currents.

14. The display device according to claim 13, wherein the plurality of gradation current transistors each transistor differs in size and each control terminal thereof is connected in parallel;

the gradation currents flow in the current path of each of the gradation current transistors.

15. The display device according to claim 14, wherein the channel width of each gradation current transistor is set at a different ratio with each other specified by 2n (n= 0, 1, 2 and 3, ...).

16. The display device according to claim 13, wherein each gradation current generation circuit comprises a reference voltage generation circuit for generating reference voltage based on the reference current.

17. The display device according to claim 16, wherein the reference voltage generation circuit comprises reference current transistors (Tr21, Tr31, Tr61) for generating reference voltage to the control terminals; the reference current is supplied to the current path;

the reference current transistor control terminals are connected in common to the control terminals of the plurality of gradation current transistors.

18. The display device according to claim 17, wherein the reference current transistors and the plurality of gradation current transistors constitute a current mirror circuit.

19. The display device according to claim 17, wherein at least any one of the reference current transistors and the plurality of gradation current transistors constitute a transistor structure which comprises:

a channel region (Rchn) in the semiconductor layer (Rac) formed by an insulator layer in the entire surface side of a semiconductor substrate (sub);

a source region (RS) and a drain region (RD) formed across the channel region (Rchn);

a terminal region (RT) formed and projected from the channel region in a vertical direction toward the opposite axis of the source region and the drain region;

a gate electrode (EG) formed by a gate insulator layer

on said channel region;

a drain electrode (ED) electrically connected to the drain region; and

a single body terminal electrode (EB) electrically connected to the source region and the terminal region.

20. The display device according to claim 1, wherein each gradation current generation circuit further comprises a reference voltage generation circuit for generating reference voltage based on the reference current.

21. The display device according to claim 20, wherein the reference voltage generation circuit comprises an electric charge storage circuit (C1) for storing the electric charge in response to the current component of the reference current.

22. The display device according to claim 1, wherein the signal driver circuit comprises:

a reference current supply line for supplying the reference current; and,

a structure in which the reference current is supplied to the plurality of gradation current generation circuits via the reference current supply line.

23. The display device according to claim 22, wherein each gradation generation circuit comprises a supply control switching

circuit (TS1, TS2) for controlling the supply state of the reference current from the reference current supply line to the proper gradation current generation circuit;

the supply control switching circuit selectively performs switching control so the reference current may be supplied only to any one gradation current circuit of the plurality of gradation current generation circuits.

24. The display device according to claim 23, wherein each current generation circuit comprises a signal holding circuit for taking in and holding the display signal.

25. The display device according to claim 24, wherein the supply control switching circuit timing of the switching control synchronizes with the timing of the signal holding circuit at the time of taking in and holding the display signal.

26. The display device according to claim 1, wherein each current generation circuit further comprises a specified state setting circuit (30A, 30B) for setting the signal lines to a specified voltage (Vbk, Vr) which makes the optical elements drive in a specified operating state when the display signal has a specified value.

27. The display device according to claim 26, wherein the drive current is generated for selecting the gradation currents

according to each of the display signal bits;

the display signal specified value is a value from which all of each of the gradation currents is non-selected from the display signals;

the specified voltage is the voltage for setting the optical elements drive in a state of lowest gradation.

28. The display device according to claim 26, wherein the specified state setting circuit comprises a specified digital value judgment section (31, 33) for judging whether or not the display signal is the specified value, and a specified voltage application section (TN32, TP34) for applying the specified voltage to the signal lines based on the judgment result by the specified digital value judgment section.

29. The display device according to claim 28, wherein the specified digital value judgment section performs judgment of whether or not said display signal is the specified value based on the logical sum of each bit value of the digital signals of the display signals.

30. The display device according to claim 1, wherein each current generation circuit further comprises a reset circuit (30A, 30B) for applying predetermined reset voltage (Vr) to the signal lines in advance of the timing which supplies the drive current to the signal lines.

31. The display device according to claim 30, wherein the reset voltage is at least the low potential voltage for discharging the electric charge stored up in the capacitative element attached to the optical elements in the display pixels, and for initializing the optical elements.

32. The display device according to claim 30, wherein the drive current is generated for selecting the gradation currents according to each of the display signal bits;

the reset voltage is applied when the display signal specified value presupposes non-selection of all of the plurality of gradation currents.

33. The display device according to claim 32, wherein the reset circuit comprises:

a specified digital value judgment section (31, 33) for judging whether or not the display signal is the specified value; and

a reset voltage application section (TN32, TP34) for applying the reset voltage to the signal lines based on the judgment result by the specified digital value judgment section.

34. The display device according to claim 33, wherein the specified digital value judgment section performs judgment of whether or not the display signal is the specified value based

on the logical sum of each bit value of the digital signals of the display signals.

35. The display device according to claim 1, wherein the optical elements in the display pixels comprise light emitting elements for accomplishing light generation operation by way of luminosity gradation according to the current value of the supply current.

36. The display device according to claim 35, wherein the light emitting elements comprise organic electroluminescent elements (OEL).

37. The display device according to claim 35, wherein the display pixels comprise at least a pixel driver circuit (DCx, DCy);

the pixel driver circuit includes a voltage holding circuit (Cx, Cy) for holding the voltage component in response to the drive current supplied from the signal driver circuit; and

a current supply circuit (Tr73, Tr81, Tr83, Tr91, Tr93, Tr103) for supplying luminescent drive current to the light emitting elements based on the voltage component held in the voltage holding circuit and for making the light emitting elements emit light.

38. The display device according to claim 37, wherein the pixel

driver circuit comprises an electric discharge circuit (Tr85) for discharging the electric charge responsive to the voltage component stored up in the voltage holding circuit.

39. The display device according to claim 37, wherein the current supply circuit comprises transistors for use of luminescent drive for supplying luminescent current to the light emitting elements,

the transistors for use of luminescent drive has a transistor structure which comprises:

in the semiconductor layer formed by an insulator layer in the entire surface side of a semiconductor substrate;

a channel region;

a source region and a drain region formed across the channel region;

a terminal region formed and projected from the channel region in a vertical direction toward the opposite axis of the source region and the drain region;

a gate electrode formed by a gate insulator layer on the channel region;

a drain electrode electrically connected to the drain region; and

a single body terminal electrode electrically connected to the source region and the terminal region.

(Display Device 2)

40. A display device for displaying image information according to display signals consisting of digital signals comprising:

a display panel (110E) comprising a plurality of signal lines (DL) and a plurality of scanning lines (SL) which intersect at right angles with each other, and a plurality of display pixels (EP, EPa) arranged near the intersecting point of the plurality of signal lines and the plurality of scanning lines comprising at least an optical element formed of the current drive type and a current generation circuit (DCz, DCz', DCza); the current generation circuit comprises a gradation current generation circuit for generating a plurality of gradation currents corresponding to each of the display signal bits based on predetermined, constant reference current; a drive current generation circuit for generating drive current based on the value of the display signal which supplies the drive current to the optical elements;

a scanning driver circuit (120C) for sequentially applying a scanning signal for setting the selective state of each line of each scanning line; and

a signal driver circuit (130H) for supplying the display signal to the plurality of signal lines.

41. The display device according to claim 40, wherein the current generation circuit further comprises a signal holding circuit which takes in the display signal and holds the signal.

42. The display device according to claim 41, wherein the current generation circuit generates said drive current based on the value of the display signal held in the holding circuit.

43. The display device according to claim 41, wherein the signal holding circuit comprises a plurality of latch circuits which take in and hold each of the display signal bits, and output an output signal responsive to each bit.

44. The display device according to claim 41, wherein the current generation circuit comprises a select switching circuit which selects the gradation current from the plurality of gradation currents responsive to each bit value of the display signal.

45. The display device according to claim 44, wherein the current generation circuit further comprises signal holding circuit which takes in the display signal and holds the signal.

46. The display device according to claim 45, wherein the signal holding circuit comprises a plurality of latch circuits which takes in and holds each bit of the display signal and outputs an output signal responsive to each bit;

the select switching circuit selects the gradation currents and generates the current drive based on the output of a plurality of latch circuits.

47. The display device according to claim 40, wherein the current value of the plurality of gradation currents have a different ratio with each other specified by 2n (n= 0, 1, 2 and 3, ...).

48. The display device according to claim 40, wherein the gradation current generation circuit comprises a plurality of gradation current transistors which generate a plurality of gradation currents.

49. The display device according to claim 48, wherein the plurality of gradation current transistors each transistor differs in size and each control terminal thereof is connected in parallel;

the gradation currents flow in the current path of each of the gradation current transistors.

50. The display device according to claim 49, wherein the channel width of each gradation current transistor is set at a different ratio with each other specified by 2n (n= 0, 1, 2 and 3, ...).

51. The display device according to claim 48, wherein each gradation current generation circuit comprises a reference voltage generation circuit for generating reference voltage based on the reference current.

52. The display device according to claim 51, wherein the

reference voltage generation circuit comprises reference current transistors for generating reference voltage to the control terminals; the reference current is supplied to the current path;

the reference current transistor control terminals are connected in common to the control terminals of the plurality of gradation current transistors.

53. The display device according to claim 52, wherein the reference current transistors and the plurality of gradation current transistors constitute a current mirror circuit.

54. The display device according to claim 52, wherein at least any one of the reference current transistors and the plurality of gradation current transistors constitute a transistor structure which comprises:

a channel region in the semiconductor layer formed by an insulator layer in the entire surface side of a semiconductor substrate;

a source region and a drain region formed across the channel region;

a terminal region formed and projected from the channel region in a vertical direction toward the opposite axis of the source region and the drain region;

a gate electrode formed by a gate insulator layer on the channel region;

a drain electrode electrically connected to the drain

region; and

a single body terminal electrode electrically connected to the source region and the terminal region.

55. The display device according to claim 40, wherein the current generation circuit further comprises a specified state setting circuit for setting the signal lines to a specified voltage which makes the optical elements drive in a specified operating state when the display signal has a specified value.

56. The display device according to claim 55, wherein the drive current is generated for selecting the gradation currents according to each bit of the display signal;

the display signal specified value is a value from which all of each of the gradation currents is non-selected from the display signals;

the specified voltage is the voltage for setting the optical elements drive in a state of lowest gradation.

57. The display device according to claim 56, wherein the specified state setting circuit comprises a specified digital value judgment section for judging whether or not the display signal is the specified value, and a specified voltage application section for applying the specified voltage to the signal lines based on the judgment result by the specified digital value judgment section.

58. The display device according to claim 40, wherein the current generation circuit further comprises a reset circuit for applying predetermined reset voltage to the optical elements in advance of the timing which supplies the drive current to the optical elements.

59. The display device according to claim 58, wherein the reset voltage is at least the low potential voltage for initializing the optical elements and discharging the electric charge stored up in the capacitative element attached to the optical elements.

60. The display device according to claim 58, wherein the drive current is generated for selecting the gradation currents according to each of the display signal bits;

the reset voltage is applied when the display signal specified value presupposes non-selection of all of the plurality of gradation currents.

61. The display device according to claim 60, wherein the reset circuit comprises a specified digital value judgment section for judging whether or not the display signal is the specified value, and a reset voltage application section for applying the reset voltage to the optical elements based on a judgment result by the specified value judgment section.

62. The display device according to claim 40, wherein the optical elements comprise light emitting elements which accomplish light generation operation by way of luminosity gradation according to the current value of the supply current.

63. The display device according to claim 62, wherein the light emitting elements are an organic electroluminescent element.

64. A method for driving the display device which displays image information according to display signals consisting of digital signals in a display panel comprising a plurality of display pixels provided with optical elements arranged close to the intersecting point of a plurality of signal lines and a plurality of scanning lines, the method comprising:

taking in and holding the display signal corresponding to the plurality of display pixels;

generating drive current according to a value of the held display signal from a plurality of gradation currents generated corresponding to each of the display signal bits based on constant, predetermined reference current; and

supplying the drive current to the plurality of signal lines.

65. The method for driving the display device according to claim 64, wherein a current value of the plurality of gradation currents have a different ratio with each other specified by 2n (n= 0,

1, 2 and 3, ...).

66. The method for driving the display device according to claim 64, wherein the generating drive current step includes selecting and integrating corresponding to the gradation currents in response to each bit value of the display signal.

67. The method for driving the display device according to claim 64, wherein the signal polarity of the drive current is set so the drive current flows in the direction drawn from the display pixels.

68. The method for driving the display device according to claim 64, wherein the signal polarity of the drive current is set so the drive current flows in the direction poured into the display pixels.

69. The method for driving the display device according to claim 64, wherein the optical elements in the display pixels comprise light emitting elements which accomplish light generation operation by way of luminosity gradation according to the current value of the supply current.

70. The method for driving the display device according to claim 69, wherein the light emitting elements comprise organic electroluminescent elements (OEL).

71. The method for driving the display device according to claim 69, further comprising:

holding the voltage component corresponding to the drive current;

supplying luminescent drive current to the light emitting elements based on the voltage component held in the voltage holding circuit, which makes the light emitting elements emit light.

72. The method for driving the display device according to claim 64, further comprising:

judging whether or not the display signal is a specified value;

applying the specified voltage which makes the display pixels drive in a specified operating state to the signal lines when judged the display signal as being the specified value.

73. The method for driving the display device according to claim 72, wherein the drive current is generated by selecting the gradation currents according to each of the display signal bits;

the specified value is a value from which all of each of the gradation currents is non-selected from the display signal;

the specified voltage is the voltage for setting the optical elements drive in a state of lowest gradation.

74. The method for driving the display device according to claim 64, further comprises applying a predetermined reset voltage to the signal lines at the timing before applying the drive current to each signal line.

75. The method for driving the display device according to claim 74, wherein the reset voltage is at least the low potential voltage for initializing each load and discharging the charge stored up in the capacitative element attached to each load.

76. The method for driving the display device according to claim 75, wherein the drive current is generated by selecting the gradation currents according to each of the display signal bits,

the reset voltage is applied when the display signal becomes the specified value which presupposes non-selection of all gradation currents.

77. The method for driving the display device according to claim 76, wherein the reset voltage applying step further comprises:

judging whether the display signal is the specified value or not,

applying the reset voltage to the signal lines when judged the display signal as being the specified value.

78. The method for driving the display device according to claim 64, further comprises discharging the charge stored up in the

capacitative element attached to the optical elements in the display pixels at the timing before applying the drive current to each signal line.